SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-179131; filed on September 11, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a semiconductor device.

BACKGROUND

Crystal defect of a semiconductor layer can cause reliability failure of a semiconductor device. For example, in a SiC device which uses a SiC substrate, stacking fault (SF) which grows from basal plane dislocation (BPD) of the SiC substrate during an operation of a device is known to cause the reliability failure of the SiC device. For this reason, it is preferable to identify a semiconductor chip whose reliability can fail while die sorting is performed to sort good devices and failed devices.

An example of related art includes JP-A-2006-349482.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic top view of a semiconductor device according to a first embodiment.

FIG. 2 is a schematic sectional view of the semiconductor device according to the first embodiment.

FIGS. 3A and 3B are schematic views of a first identification mark according to the first embodiment.

FIGS. 4A and 4B are schematic views of a second identification mark according to the first embodiment.

FIGS. 5A and 5B are explanatory views of a test method of the semiconductor device according to the first embodiment.

FIGS. 6A and 6B are schematic views of a first identification mark and a second identification mark according to a second embodiment.

FIGS. 7A and 7B are schematic views of a first identification mark and a second identification mark according to a third embodiment.

DETAILED DESCRIPTION

[0004]Exemplary embodiments provide a semiconductor device which can reduce reliability failure.

[0005]In general, according to one embodiment, a semiconductor device includes a first identification mark which is identifiable by using a photoluminescence method; and a second identification mark which is identifiable by using visible light.

[0007]Hereinafter, exemplary embodiments will be descried with reference to the drawings. In the following description, the same symbols or reference numerals will be attached to the same or similar members or the like, and description of the members or the like described once will be appropriately omitted.

[0008]In addition, in the following description, notation of n+, n and n-, and p+, p and p- represents relative levels of impurity concentrations of each conductive type. That is, it represents that n+-type impurity concentration is relatively higher than n-type impurity concentration, and n--type impurity concentration is relatively lower than n-type impurity concentration. In addition, it represents that p+-type impurity concentration is relatively higher than p-type impurity concentration, and p--type impurity concentration is relatively lower than p-type impurity concentration. There is a case in which n+ and n- are simply described as an n type, and p+ and p- are simply described as a p type.

First Embodiment

[0009]A semiconductor device according to the present embodiment includes a first identification mark which is identifiable by using a photoluminescence method, and a second identification mark which is identifiable by using visible light.

[0010]FIG. 1 is a schematic top view of a semiconductor device according to the present embodiment. FIG. 2 is a schematic sectional view of the semiconductor device according to the present embodiment. FIG. 2 is a cross-sectional view taken along line II-II. The semiconductor device according to the present embodiment is a PIN diode which uses a SiC substrate.

[0011]The PIN diode 100 includes an element region 100a, a termination region 100b, a dicing region 100c, a first identification mark 110, and a second identification mark 120. The element region 100a is surrounded by the termination region 100b. The termination region 100b is surrounded by the dicing region 100c.

[0012]The element region 100a functions as a region through which a current mainly flows at the time of a forward bias of the PIN diode 100.

[0013]The termination region 100b functions as an area in which strength of an electric field that is applied to an end portion of the element region 100a is reduced at the time of a reverse bias of the PIN diode 100, and a breakdown voltage of an element of the PIN diode 100 increases. The termination region 100b has, for example, a RESURF structure or a guide ring structure.

[0014]The dicing region 100c is a planned cutting region which is used for dividing a semiconductor layer into a plurality of semiconductor chips. In the present specification, a portion of the dicing region 100c remaining in the semiconductor chip after being cut is also simply referred to as the dicing region 100c.

[0015]The first identification mark 110 and the second identification mark 120 are provided in a region between the termination region 100b and the dicing region 100c. In other words, the first identification mark 110 and the second identification mark 120 are provided in a region which is provided such that a termination region 100b is interposed between the element region 100a and the region.

[0016]The PIN diode 100 includes a semiconductor layer 10, a base oxide film (first insulating film) 12, an interlayer insulating film (second insulating film) 14, an anode electrode 16, and a cathode electrode 18. An n+-type cathode region 20, an n--type drift region 22, a p-type anode region 24, a p--type RESURF region 25, and a p-type guide ring region 26 are provided in the semiconductor layer 10.

[0017]The p-type anode region 24 is provided in the element region 100a. The p--type RESURF region 25 is provided in the termination region 100b. The p--type RESURF region 25 is provided in a ring shape so as to surround the p-type anode region 24. The p--type RESURF region 25 comes into contact with the p-type anode region 24. The p--type RESURF region 25 contains lower p-type impurity concentration than that of the p-type anode region 24. The p-type guide ring region 26 is provided in the termination region 100b. A plurality of p-type guide ring regions 26 are provided, and each of the p-type guide ring regions 26 has a ring shape.

[0018]The semiconductor layer 10 is a semiconductor with a wider bandgap than that of silicon. The semiconductor layer 10 is, for example, a SiC layer with a 4H-SiC structure. A thickness of the semiconductor layer 10 is, for example, greater than 5 mm and smaller than 600 mm.

[0019]The base oxide film 12 is, for example, a thermal oxide film. The base oxide film 12 is, for example, a silicon oxide film.

[0020]The interlayer film 14 is a deposited film which is formed by using, for example, a chemical vapor deposition (CVD) method. The interlayer film 14 is, for example, a silicon oxide film.

[0021]The first identification mark 110 is a mark which is identifiable by using a photoluminescence method (PL method). The photoluminescence method is a method of observing light occurring when a material is irradiated with light and excited electrons transitions to a ground state. For example, ultraviolet laser is used as the excited light. It is possible to evaluate, for example, crystal defect of single crystal, or impurity, using a photoluminescence method.

[0022]FIGS. 3A and 3B are schematic views of a first identification mark according to the present embodiment. FIG. 3A is a top view, and FIG. 3B is a cross-sectional view taken along line IIIB-IIIB of FIG. 3A.

[0023]The first identification mark 110 includes, for example, a character string as illustrated in FIG. 3A. An one-dimensional or two-dimensional bar code can also be applied to the first identification mark 110, in addition to the character string.

[0024]The first identification mark 110 includes an amorphous SiC region (amorphous region) 110a. The amorphous SiC region 110a is provided in the semiconductor layer 10. The amorphous SiC region 110a is formed so as to become, for example, a pattern of a character string.

[0025]For example, the amorphous SiC region 110a can be formed by selectively injecting argon (Ar) into the semiconductor layer 10, using an ion injection method. In addition, for example, the amorphous SiC region 110a can be formed by selectively irradiating the semiconductor layer 10 with an electron beam.

[0026]As the amorphous SiC region 110a is provided in the semiconductor layer 10, the amorphous SiC region 110a emits light by using a photoluminescence method, and thereby the first identification mark 110 is identifiable.

[0027]It doesn’t matter that a polycrystalline SiC region (polycrystalline) is provided in addition to the amorphous SiC region 110a. It doesn’t matter that the amorphous SiC region 110a is, for example, a p-type impurity region formed by ion-injection of p type impurity such as aluminum (Al), or an n-type impurity region formed by ion-injection of n-type impurity such as nitride (N).

[0028]The second identification mark 120 is a mark which is identifiable by using visible light. The visible light is, for example, light with a wavelength longer than or equal to 380 nm and shorter than or equal to 780 nm.

[0029]FIGS. 4A and 4B are schematic views of a second identification mark according to the present embodiment. FIG. 4A is a top view, and FIG. 4B is a cross-sectional view taken along line IVB-IVB of FIG. 4A.

[0030]The second identification mark 120 includes, for example, a character string as illustrated in FIG. 4A. An one-dimensional or two-dimensional bar code can also be applied to the second identification mark 120, in addition to the character string.

[0031]The second identification mark 120 includes a metal region 120a. The metal region 120a is provided on the interlayer film 14. The metal region 120a is formed so as to become, for example, a pattern of a character string.

[0032]For example, the metal region 120a can be formed by patterning a metal film formed on the interlayer film 14. The metal region 120a can be formed at the same time as, for example, the anode electrode 16.

[0033]By providing the metal region 120a, it is possible to identify the second identification mark 120, using visible light.

[0034]In the present embodiment, the first identification mark 110 and the second identification mark 120 have the same pattern. However, other patterns can also be employed on the assumption that mapping of the first identification mark 110 and the second identification mark 120 is made.

[0035]Next, a test method of the semiconductor device according to the present embodiment will be described with reference to FIG. 1 to FIG. 5B. In the test method of the semiconductor device according to the present embodiment, a plurality of first identification marks, which are different from each other and is identifiable by using a photoluminescence method, are formed in a semiconductor layer; a plurality of second identification marks which are different from each other and is identifiable by using visible light, are formed on the semiconductor layer; a crystal defect test is performed for the semiconductor layer, using the photoluminescence method; mapping of crystal defects detected by the crystal defect test and the first identification mark identified by using the photoluminescence method, is made; and the second identification mark corresponding to the first identification mark is identified by using visible light, and thereby, a semiconductor chip having the first identification mark mapped with the crystal defects is determined to be a failed product.

[0036]FIGS. 5A and 5B are explanatory views of a test method of the semiconductor device according to the present embodiment. FIGS. 5A and 5B illustrate a state shortly before die sorting of a semiconductor device which is tested by the test method of the semiconductor device according to the present embodiment. FIG. 5A is a top view of the semiconductor device, and FIG. 5B is an enlarged view of a partial region of FIG. 5A.

[0037]For example, a plurality of semiconductor chips are formed on the semiconductor layer 10. Each semiconductor chip is the PIN diode 100. The plurality of semiconductor chips are disposed in a matrix in a state in which include the dicing region 100c is interposed between the plurality of semiconductor chips.

[0038]FIG. 5A illustrates a pattern corresponding to one shot when the pattern is formed on the semiconductor layer 10 by using a step-and-repeat method of lithography. That is, in the present embodiment, a pattern of 20 chips can be formed by one shot.

[0039]First, the semiconductor layer 10 including the n+-type cathode region 20 and the n--type drift region 22 is prepared. The semiconductor layer 10 is a 4H-SiC substrate.

[0040]Subsequently, a pattern of the first identification mark 110 is formed on the semiconductor layer 10. For example, the base oxide film 12 is formed by performing thermal oxidation of the semiconductor layer 10.

[0041]Subsequently, patterning of a photoresist film is performed into a pattern corresponding to the first identification mark 110, using a lithography method. At this time, 20 chips which are formed by one shot include the first identification mark 110 which are different from each other.

[0042]Subsequently, ion injection of argon (Ar) is performed by using the photoresist as a mask, and the amorphous SiC region 110a is formed.

[0043]Thereafter, a crystal defect test of the semiconductor layer 10 is performed by using the photoluminescence method. For example, if crystal defect which can cause reliability failure is discovered, the first identification mark 110 of a chip corresponding to the crystal defect is identified by using the photoluminescence method. The first identification mark 110 of the chip in which the crystal defect is discovered is stored.

[0044]Thereafter, the p-type anode region 24, the p--type RESURF region 25, the p-type guide ring region 26, and the anode electrode 16 are formed by using the known process technology.

[0045]When the anode electrode 16 is formed, a pattern of the second identification mark 120 is formed at the same time. That is, the second identification mark 120 is formed by patterning the metal region 120a. The 20 chips which are formed by one shot includes the second identification marks 120, each being mapped with and different from the first identification mark 110.

[0046]Thereafter, the cathode electrode 18 is formed by using the known process technology.

[0047]Subsequently, die sorting, which sorts good products and failed products of the plurality of semiconductor devices that are fabricated, is performed. At the time of die sorting, for example, the second identification marks 120 of each semiconductor chip are read by using visible light. A semiconductor chip, which includes the second identification mark 120 corresponding to the first identification mark 110 of a chip in which crystal defect causing reliability failure is discovered, is determined to be a failed product.

[0048]After the die sorting, the semiconductor layer 10 is cut along the dicing region 100c by using, for example, a dicing blade, and thereby a plurality of semiconductor chips are diced.

[0049]Sorting the failed products by reading the second identification marks 120 of each semiconductor chip using visible light can also be performed after the plurality of semiconductor chips are diced.

[0050]Next, actions and effects of the present embodiment will be described.

[0051]Crystal defect of a semiconductor layer can cause reliability failure of a semiconductor device. For example, in a SiC substrate, a BPD included in the SiC substrate is propagated into the SiC layer, when epitaxial growth of the SiC layer is performed on the SiC substrate. BPD which reaches the surface of the SiC layer among the BPD propagated into the SiC layer is expanded by an operation of the semiconductor device. Expanded SF causes reliability failure of variation of an ON voltage or the like. However, the reliability is hardly identified by electrical evaluation shortly after the semiconductor device is fabricated.

[0052]A line defect such as BPD among crystal defects which can cause reliability failure cannot be discovered in the test which uses visible light. However, the defect can be discovered by crystal defect test which uses a photoluminescence method, for example, before fabrication of the semiconductor chip, or during the fabrication. However, since a plurality of semiconductor chips are formed in the semiconductor layer, mapping of the discovered crystal defect and the semiconductor chips is hardly made.

[0053]For example, it is considered that mapping is made by using positional information of a stage on which a semiconductor layer is mounted. However, in this method, particularly, sufficient accuracy cannot be obtained if a size of the semiconductor chip decreases, and mapping is hardly made.

[0054]In the present embodiment, the first identification mark 110 which is identifiable by using the photoluminescence method is provided in semiconductor chip. The first identification marks 110 become different between the plurality of semiconductor chips formed in the semiconductor layer.

[0055]Hence, it is possible to make mapping of crystal defects which are discovered by the crystal defect test which uses the photoluminescence method before the fabrication of the semiconductor chip or during the fabrication, with a specified semiconductor chip by using the first identification mark 110.

[0056]Furthermore, it is possible to easily identify the specified semiconductor chip which is a failed product after the semiconductor chip is fabricated, using the second identification mark 120 which is identifiable by using visible light and in which mapping with the first identification mark 110 is made.

[0057]According to the semiconductor device according to the present embodiment, it is possible to sort a semiconductor chip which can result in reliability failure due to crystal defects, as a failed product. Hence, it is possible to provide a semiconductor device which can reduce reliability failure.

Second Embodiment

[0058]A semiconductor device according to the present embodiment is the same as the semiconductor device according to the first embodiment except that the second identification mark includes a partial region of the second insulating film provided between the first insulating films on the semiconductor layer with a wider bandgap than that of silicon, and the first identification mark includes an amorphous region, polycrystalline region, and an n-type impurity region or a p-type impurity region. Hence, description of contents which overlap those of the first embodiment will be omitted.

[0059]FIGS. 6A and 6B are schematic views of the first identification mark and the second identification mark according to the second embodiment. FIG. 6A is a top view, and FIG. 6B is a cross-sectional view taken along line VIB-VIB of FIG. 6A.

[0060]In the present embodiment, the first identification mark 110 and the second identification mark 120 are provided in the same position in a planar view.

[0061]The first identification mark 110 and the second identification mark 120 include, for example, character strings, as illustrated in FIG. 6A. In addition to the character string, an one-dimensional or two-dimensional bar code can also be applied to the first identification mark 110.

[0062]The first identification mark 110 includes a p-type SiC region (p-type impurity region) 110b which contains p-type impurity. The p-type impurity is, for example, aluminum (Al).

[0063]The p-type SiC region 110b is provided in the semiconductor layer 10. The p-type SiC region 110b is formed so as to be a pattern of, for example, a character string.

[0064]By providing the p-type SiC region 110b in the semiconductor layer 10 of single crystal, the p-type SiC region 110b emits light using the photoluminescence method, and the first identification mark 110 is identifiable.

[0065]The second identification mark 120 includes a partial region 14a of the interlayer insulating film (second insulating film) 14 which is interposed between the base oxide films (first insulating film) 12 that is provided on the semiconductor layer 10. The partial region 14a is formed so as to be a pattern of, for example, a character string.

[0066]Roughness is formed on an upper surface of the region 14a of the interlayer insulating film 14. Since roughness is formed on the upper surface of the region 14a, it is possible to identify the second identification mark 120, using visible light.

[0067]The p-type SiC region 110b is provided in the semiconductor layer 10 under the region 14a.

[0068]The first identification mark 110 and the second identification mark 120 can be formed by using the following method.

[0069]First, the base oxide film 12 is formed on the semiconductor layer 10. Subsequently, patterning of a photoresist film is performed in a pattern corresponding to the first identification mark 110 by using a lithography method.

[0070]Ion injection of p-type impurity into the semiconductor layer 10 is performed by using the patterned base oxide film 12 as a mask, and the p-type SiC region 110b is formed in the semiconductor layer 10 under a groove portion of the base oxide film 12.

[0071]Subsequently, the interlayer insulating film 14 is laminated on the base oxide film 12. The groove portion of the base oxide film 12 is filled with the interlayer insulating film 14. The groove portion of the base oxide film 12 filled with the interlayer insulating film 14 becomes the region 14a. Roughness is formed on an upper surface of the region 14a of the interlayer insulating film 14.

[0072]In addition to the p-type SiC region 110b, an n-type SiC region (n-type impurity region) containing n-type impurity can also be applied. In addition, in addition to the p-type SiC region 110b, an amorphous SiC region (amorphous region) or a polycrystalline SiC region (polycrystalline region) can also be applied.

[0073]According to the semiconductor device according to the present embodiment, in the same manner as in the first embodiment, it is possible to sort a semiconductor chip which can result in reliability failure due to crystal defects, as a failed product. Hence, it is possible to provide a semiconductor device which can reduce reliability failure.

[0074]In addition, the first identification mark 110 and the second identification mark 120 are provided in the same position in a planar view. For this reason, it is possible to reduce an area necessary for providing the first identification mark 110 and the second identification mark 120. In addition, the first identification mark 110 and the second identification mark 120 are easily formed.

Third Embodiment

[0075]A semiconductor device according to the present embodiment is the same as the semiconductor device according to the first embodiment except for the second identification mark includes a concave portion provided on a surface of a semiconductor layer, and the first identification mark includes an amorphous region, a polycrystalline region, an n-type impurity region or a p-type region which is provided in a semiconductor layer under the concave portion. Hence, description of contents which overlap those of the first embodiment will be omitted.

[0076]FIGS. 7A and 7B are schematic views of the first identification mark and the second identification mark according to the present embodiment. FIG. 7A is a top view, and FIG. 7B is a cross-sectional view taken along line VIIB-VIIB of FIG. 7A.

[0077]In the present embodiment, the first identification mark 110 and the second identification mark 120 are provided in the same position in a planar view.

[0078]The first identification mark 110 and the second identification mark 120 include, for example, character strings, as illustrated in FIG. 7A. In addition to the character string, an one-dimensional or two-dimensional bar code can also be applied to the first identification mark 110.

[0079]The first identification mark 110 includes a p-type SiC region (p-type impurity region) 110b which contains p-type impurity. The p-type impurity is, for example, aluminum (Al).

[0080]The p-type SiC region 110b is provided in the semiconductor layer 10. The p-type SiC region 110b is formed so as to be a pattern of, for example, a character string.

[0081]By providing the p-type SiC region 110b in the semiconductor layer 10 of single crystal, the p-type SiC region 110b emits light using the photoluminescence method, and the first identification mark 110 is identifiable.

[0082]The second identification mark 120 includes a concave portion (groove) 15 which is provided on a surface of the semiconductor layer 10. The concave portion 15 is formed so as to be a pattern of, for example, a character string.

[0083]Roughness is formed on the surface of the semiconductor layer 10 and an upper surface of the base oxide film 12. Since roughness is formed on the surface of the semiconductor layer 10 and the upper surface of the base oxide film 12, it is possible to identify the second identification mark 120, using visible light.

[0084]The p-type SiC region 110b is provided in the semiconductor layer 10 under the concave portion 15.

[0085]In the present embodiment, for example, an interlayer insulating film is not provided on the base oxide film 12.

[0086]The first identification mark 110 and the second identification mark 120 can be formed by using the following method.

[0087]First, a mask member is formed on the semiconductor layer 10. The mask member is, for example, a silicon oxide film. Subsequently, patterning of a photoresist film is performed on the mask member in a pattern corresponding to the first identification mark 110 by using a lithography method.

[0088]Subsequently, patterning of the mask member is performed by reactive ion etching (RIE). Subsequently, the photoresist film is removed.

[0089]Subsequently, the semiconductor layer 10 is etched by the RIE, using the mask member as a mask, and the concave portion 15 is formed. Subsequently, ion injection of p type impurity into the semiconductor layer 10 is performed by using the mask member as a mask, and the p-type SiC region 110b is formed in the semiconductor layer 10 under the concave portion 15.

[0090]Subsequently, the mask member is removed, and the base oxide film 12 is formed by thermal oxidation. Roughness is formed on the surface of the semiconductor layer 10 and the upper surface of the base oxide film 12.

[0091]In addition to the p-type SiC region 110b, an n-type SiC region (n-type impurity region) containing n-type impurity can also be applied. In addition, in addition to the p-type SiC region 110b, an amorphous SiC region (amorphous region) or a polycrystalline SiC region (polycrystalline region) can also be applied.

[0092]In addition, in the present embodiment, a case in which the concave portion 15 is formed on the surface of the semiconductor layer 10 and the concave portion 15 is used for the second identification mark 120 is used as an example, but, for example, it is possible that the concave portion 15 is not provided on the surface of the semiconductor layer 10, the mask member which is used as a mask of ion injection is left without being removed, and the roughness of the mask member is used for the second identification mark 120.

[0093]According to the semiconductor device according to the present embodiment, in the same manner as in the first embodiment, it is possible to sort a semiconductor chip which can result in reliability failure due to crystal defects, as a failed product. Hence, it is possible to provide a semiconductor device which can reduce reliability failure.

[0094]In addition, the first identification mark 110 and the second identification mark 120 are provided in the same position in a planar view. For this reason, it is possible to reduce an area necessary for providing the first identification mark 110 and the second identification mark 120. In addition, the first identification mark 110 and the second identification mark 120 are easily formed.

[0095]In the first to third embodiments, a case in which the first identification mark 110 and the second identification mark 120 are provided between the termination region 100b and the dicing region 100c is used as an example, but the first identification mark 110 and the second identification mark 120 can also be provided in the dicing region 100c. This form is effective in a case space for providing the first identification mark 110 and the second identification mark 120 is not able to be ensured in a semiconductor chip.

[0096]In the first to third embodiments, the PIN diode is used as an example, but exemplary embodiments can be applied to other devices, such as, a Schottky barrier diode, a metal oxide semiconductor field effect transistor (MOSFET), a metal insulator semiconductor field effect transistor (MISFET), or an insulated gate bipolar transistor (IGBT).

[0097]While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of exemplary embodiments. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first identification mark which is identifiable by using a photoluminescence method; and

a second identification mark which is identifiable by using visible light.

2. The device according to Claim 1, wherein the first identification mark includes an amorphous region or a polycrystalline region which is provided in a semiconductor layer with a wider bandgap than a bandgap of silicon.

3. The device according to Claim 1, wherein the first identification mark includes an n-type impurity region or a p-type impurity region which is provided in a semiconductor layer with a wider bandgap than a bandgap of silicon.

4. The device according to any one of Claims 1 to 3, wherein the first identification mark and the second identification mark are provided in a region which is provided such that a termination region which surrounds an element region is interposed between the element region and the region.

5. The device according to any one of Claims 2 to 5, wherein the semiconductor layer is a SiC layer.

ABSTRACT

According to one embodiment, a semiconductor device includes a first identification mark which is identifiable by using a photoluminescence method; and a second identification mark which is identifiable by using visible light.